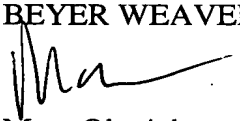
REMARKS

Claims 7, 54, and 58 have been amended. New claim 107 has been added. Accordingly, claims 7, 54-60, and 107 remain pending. The amendments and new claim do not add any new matter. For example, the amendments are supported within the specification on page 43, lines 25-29 and page 44, lines 1-27, among other places.

The Examiner has rejected claims 7 and 54-60 under 35 U.S.C. §112, second paragraph, as being indefinite because the scope of the term "adding dummy fillings within a top conductive layer of the plurality of conductive layer so as to minimize defects" in claim 7 and the term "forming a plurality of dummy fillings that are positioned and sized to minimize..." of claim 54 is unclear. Claims 7 and 54 have been amended to clarify the invention. For example, claims 7 and 54 now require "providing a semiconductor die having a plurality of first areas which are specified by a design as containing structures selected from a group consisting of a product structure and a test structure" and "determining whether one or more empty spaces that are positioned outside the first areas require dummy fillings to facilitate an even polishing of a surface of the semiconductor die during CMP polishing." It is respectfully submitted that those skilled in the art would know how to determine which empty spaces require dummy filling to facilitate an even polishing. By way of example, one may determine this by consideration of size configuration of the empty spaces and/or use of commonly availably software. See page 44, lines 15-17 of the Specification. Accordingly, it is respectfully submitted that all pending claims meet the requirements under 35 U.S.C. §112, second paragraph.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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APPENDIX:

MARKED UP VERSION OF SPECIFICATION AND CLAIM AMENDMENTS

Claims 7 and 54 have been amended as follows:

7. (Amended Once) A method of fabricating a semiconductor die, comprising:

providing a semiconductor die having a plurality of first areas which are specified by a design as containing structures selected from a group consisting of a product structure and a test structure;

determining whether one or more empty spaces that are positioned outside the first areas require dummy fillings to facilitate an even polishing of a surface of the semiconductor die during CMP polishing;

forming a plurality of conductive layers within at least one of the empty spaces which are determined to require dummy fillings so as to form a test structure, wherein a top conductive layer of the plurality of conductive layers within the at least one of the empty spaces which are determined to require dummy fillings includes a dummy filling coupled to the test structure.[;

forming a test structure from at least one of the plurality of conductive layers; and

adding dummy fillings within a top conductive layer of the plurality of conductive layers so as to minimize defects from CMP, wherein at least one of the dummy filling is formed over the test structure.]

54. (Amended Once) A method of fabricating a test structure on a semiconductor die, comprising:

providing a semiconductor die having a plurality of first areas which are specified by a design as containing structures selected from a group consisting of a product structure and a test structure;

determining whether one or more empty spaces that are positioned outside the first areas require dummy fillings to facilitate an even polishing of a surface of the semiconductor die during CMP polishing;

[forming a test structure; and]

forming a plurality of dummy fillings within the empty spaces determined to require dummy fillings [that are positioned and sized to minimize defects during chemical mechanical polishing, at least one of the dummy fillings being coupled to the test structure]; and

forming a test structure from at least a portion of at least one of the dummy filling.

58. (Amended Once) A method as recited in claim 56, further comprising performing voltage contrast [testing] inspection on the dummy fillings to detect a defect, wherein a defect is detected when the at least one dummy filling coupled to the test structure does not have a voltage potential that differs from a voltage potential of the other non-coupled dummy fillings.